

Claims

We claim:

1. A structure, comprising:

a fuse bay including a fuse array of N fuses, N being an integer;

a BIST circuit electrically coupled to the fuse bay;

a memory module electrically coupled to the fuse bay and the BIST circuit; and

a new repair circuit electrically coupled to the fuse bay and the BIST circuit, wherein

the fuse bay is configured to store and shift an original combined repair solution to the BIST circuit,

the BIST circuit is configured to (i) perform a first test run on the memory module so as to obtain a first test-run repair solution, and then (ii) combine the first test-run repair solution and the original combined repair solution from the fuse bay so as to obtain a first combined repair solution,

the new repair circuit is configured to receive and compare the original combined repair solution and the first combined repair solution to obtain a first new repair solution, and

the fuse bay is further configured to program the first new repair solution into the fuses of the fuse array so that the fuse bay stores the first combined repair solution.

1 2. The structure of claim 1, wherein

2 the fuse bay is further configured to shift the first combined repair solution to the BIST
3 circuit,

4 the BIST circuit is further configured to (i) perform a second test run on the memory
5 module so as to obtain a second test-run repair solution, and then (ii) combine the second test-run
6 repair solution and the first combined repair solution from the fuse bay so as to obtain a second
7 combined repair solution,

8 the new repair circuit is further configured to receive and compare the first combined
9 repair solution and the second combined repair solution to obtain a second new repair solution,
10 and

11 the fuse bay is further configured to program the second new repair solution into the fuses
12 of the fuse array so that the fuse bay stores the second combined repair solution.

1 3. The structure of claim 1, wherein the fuse bay further comprises a fuse register including N
2 fuse latches electrically coupled one-by-one to the N fuses of the fuse array, wherein the fuse
3 register is configured to obtain a copy of a content of the fuse array.

1 4. The structure of claim 1, wherein the fuse bay further comprises a program register including
2 N program latches electrically coupled one-by-one to the N fuses of the fuse array, wherein the
3 program register is configured to store a content to be programmed into the fuse array.

1 5. The structure of claim 1, wherein the new repair circuit comprises an exclusive-OR gate.

1 6. The structure of claim 1, wherein the BIST circuit comprises a repair register of N bits
2 configured to store one of the repair solutions at a time.

1 7. The structure of claim 1, wherein the number of fuses of the fuse array equals the length in bits
2 of the first test-run repair solution.

1 8. The structure of claim 1, wherein the fuses are electronically blown fuses.

1 9. A memory chip, comprising:

2 at least a memory module;

3 a fuse register electrically coupled to the memory module;

4 a fuse array electrically coupled to the fuse register, the fuse array including a plurality of
5 fuses;

6 a program register electrically coupled to the fuse array;

7 a fuse controller electrically coupled to the fuse register and the program register;

8 a BIST circuit electrically coupled to the fuse register and the fuse controller; and

9 a new repair circuit electrically coupled to the BIST circuit, the fuse register, and the
10 program register, wherein

11 the fuse array is configured to store an original combined repair solution,

12 the fuse controller is configured to cause the fuse array to send the original combined
13 repair solution to the fuse register, and then cause the fuse register to send the original combined
14 repair solution to the BIST circuit,

15 the BIST circuit is configured to (i) perform a first test run on the memory module so as
16 to obtain a first test-run repair solution, and then (ii) combine the first test-run repair solution and
17 the original combined repair solution so as to obtain a first combined repair solution,

18 the new repair circuit is configured to receive and compare the original combined repair
19 solution and the first combined repair solution to obtain a first new repair solution, and

20 the fuse controller is further configured to cause the program register to receive the first
21 new repair solution from the new repair circuit and then cause the fuse array to program the first
22 new repair solution into its fuses so that the fuse array stores the first combined repair solution.

1 10. The structure of claim 9, wherein

2 the fuse controller is further configured to cause the fuse array to send the first combined
3 repair solution to the fuse register, and then cause the fuse register to send the first combined
4 repair solution to the BIST circuit,

5 the BIST circuit is further configured to (i) perform a second test run on the memory
6 module so as to obtain a second test-run repair solution, and then (ii) combine the second test-run
7 repair solution and the first combined repair solution so as to obtain a second combined repair
8 solution,

9 the new repair circuit is further configured to receive and compare the first combined
10 repair solution and the second combined repair solution to obtain a second new repair solution,
11 and

12 the fuse controller is further configured to cause the program register to receive the
13 second new repair solution from the new repair circuit and then cause the fuse array to program

14 the second new repair solution into its fuses so that the fuse array stores the second combined
15 repair solution.

1 11. The structure of claim 9, wherein the new repair circuit comprises an exclusive-OR gate.

1 12. The structure of claim 9, wherein the fuses are electronically blown fuses.

1 13. A method for performing test runs and repairs of a memory module, the method comprising
2 the steps of:

3 using a fuse bay, including a fuse array of N fuses, N being an integer, to store and shift
4 an original combined repair solution to a BIST circuit;

5 using the BIST circuit to (i) perform a first test run on the memory module so as to obtain
6 a first test-run repair solution, and then (ii) combine the first test-run repair solution and the
7 original combined repair solution from the fuse bay so as to obtain a first combined repair
8 solution;

9 using a new repair circuit to receive and compare the original combined repair solution
10 and the first combined repair solution to obtain a first new repair solution; and

11 further using the fuse bay to program the first new repair solution into the fuses of the
12 fuse array so that the fuse bay stores the first combined repair solution.

1 14. The method of claim 13, further comprising the steps of:

2 using the fuse bay to shift the first combined repair solution to the BIST circuit;

3 using the BIST circuit to (i) perform a second test run on the memory module so as to
4 obtain a second test-run repair solution, and then (ii) combine the second test-run repair solution
5 and the first combined repair solution from the fuse bay so as to obtain a second combined repair
6 solution;

7 using the new repair circuit to receive and compare the first combined repair solution and
8 the second combined repair solution to obtain a second new repair solution; and

9 using the fuse bay to program the second new repair solution into the fuses of the fuse
10 array so that the fuse bay stores the second combined repair solution.

1 15. The method of claim 13, wherein the step of using the fuse array to store and shift the
2 original combined repair solution to the BIST circuit comprises the steps of:

3 providing in the fuse bay a fuse register including N fuse latches electrically coupled one-
4 by-one to the N fuses of the fuse array; and

5 using the fuse register to obtain a copy of a content of the fuse array.

1 16. The method of claim 13, wherein the step of using the fuse bay to program the first new
2 repair solution into the fuses of the fuse array comprises the steps of:

3 providing in the fuse bay a program register including N program latches electrically
4 coupled one-by-one to the N fuses of the fuse array; and

5 using the program register to receive the first new repair solution from the new repair
6 circuit.

1 17. The method of claim 13, wherein the new repair circuit comprises an exclusive-OR gate.

1 18. The method of claim 13, wherein the step of using the BIST circuit to perform the first test
2 run on the memory module so as to obtain the first test-run repair solution comprises the steps of:

3 providing a repair register of N bits; and

4 using the repair register to store the first test-run repair solution.

1 19. The method of claim 13, wherein the number of fuses of the fuse array equals the length in
2 bits of the first test-run repair solution.

1 20. The method of claim 13, wherein the fuses are electronically blown fuses.